



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/774,099	01/31/2001	Yasuo Onishi	010093	1075
38834	7590	12/31/2003	EXAMINER	
WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP 1250 CONNECTICUT AVENUE, NW SUITE 700 WASHINGTON, DC 20036			NELSON, ALECIA DIANE	
		ART UNIT		PAPER NUMBER
		2675		8

DATE MAILED: 12/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/774,099	ONISHI ET AL.
Examiner	Art Unit	
	Alecia D. Nelson	2675

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 17 September 2003.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-8 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 7 and 8 is/are allowed.

6) Claim(s) 1-6 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) The translation of the foreign language provisional application has been received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) Paper No(s). ____ .
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) Notice of Informal Patent Application (PTO-152)
3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____ . 6) Other: ____ .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. **Claims 1-6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Koike (EP 0 953 963).

With reference to **claims 1 and 3**, Koike discloses a display device comprising a clock generation circuit for generating sampling clocks, whose frequency is controlled on the basis of a required frequency control value, on the basis of a horizontal synchronizing signal of an input video signal (see column 7, lines 45-50); an analog-to-digital converter for sampling the input video signal on the basis of the sampling clocks

generated from the clock generation circuit (see column 6, lines 40-43); horizontal video start position detection mean for detecting a horizontal video start position of video data outputted from the analog-to-digital converter on the basis of a first threshold value, and a horizontal video end position detection means for detecting a horizontal video end position of the video data outputted from the analog-to-digital converter on the basis of a second threshold value (see column 8, lines 23-37); calculation means calculating the number of sampling clocks corresponding to the distance from the horizontal video start position to the horizontal video end position (see column 8, line 4-column 9, line 9); judgment means for judging whether or not the result of the calculation by the calculation means coincides with a required reverence value (see column 9, lines 9-19); frequency control value adjustment means for calculating, when it is judge that the result of the calculation by the calculation means and the reference value do not coincide with each other, a new frequency control value on the basis of the result of the calculation by the calculation means, the reference value, and the frequency control value currently set in the clock generation circuit, to feed the new frequency control value to the clock generation circuit (see column 9, line 51-column 10, line 1).

With further reference to the threshold value control means for controlling a second threshold value depending on the level of the video data outputted from the analog-to-digital converter, Koike teaches that the horizontal image start/end detection circuit detects a horizontal image start position (HS) and a horizontal image end position (HE) on the basis of the data outputted from the A/D converters (2R, 2G, 2B), wherein the threshold value is set to be a larger or smaller than the predetermined threshold

value, in which the smaller value is to be set slightly larger than the value of the noises in order to prevent these noises as being read as data (see column 8, lines 23-43).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for such a threshold circuit, as suggest by Koike, in the disclosed system in order to thereby provide a method and apparatus for controlling the threshold value based on the level of the video data in order to avoid problems with noise in the video data.

With reference to **claims 2 and 4**, Koike teaches that the clock generation circuit further includes a voltage controlled oscillator (43), for outputting the sampling clocks, a frequency divider (44), for dividing the frequency of the sampling clocks outputted from the VCO (43), a phase detection means, to which an output of the frequency divider and the horizontal synchronizing signal of the input video signal are inputted, for outputting a detection signal corresponding to the phase difference between both the inputted signals, a filter means for integrating the detection signal outputted from the phase detection means to output the integrated detection signal to the VCO (43), and the frequency division ratio of the frequency divider being used as the frequency control value (see column 8, lines 6-37).

With reference to **claims 5 and 6**, Koike teaches a pixel corresponding display device comprising a clock generation circuit for generating sampling clocks, whose frequency is controlled on the basis of a required frequency control value, on the basis

of a horizontal synchronizing signal of an input video signal (see column 7, lines 45-50); an A/D converter for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit (see column 6, lines 40-43); calculation means for calculating, on the basis of a horizontal video start position closest to a horizontal period start position specified by the horizontal synchronizing signal out of horizontal video start positions detected within one field and a horizontal video end position detected within one field (see column 11, lines 29-41), the number of sampling clocks corresponding to the distance between the horizontal video start position and the horizontal video end position of the input video signal for the field; frequency adjustment means for controlling the clock generation circuit on the basis of the result of the calculation by the calculation means to adjust the frequency of the sampling clocks (see column 11, lines 50-57), judgment means for judging for each field whether or not the width of a region where input video exists is smaller than the number of horizontal effective pixels on the basis of the result of the calculation by the calculation means (see column 13, lines 54-column 14, line 12).

With reference to the means/circuit for stopping, when it is judged that the width of the region where the input video exists is smaller than the number of horizontal effective pixels, a frequency adjustment operation based on the number of sampling clocks found in the field, Koike teaches a sampling clock control circuit (30) constituted by a PLL circuit (40), a total-of-horizontal dots detection circuit (50), and a phase control circuit (60), wherein the a total-of-horizontal dots detection circuit (50) comprises a horizontal image start/end detection circuit (51), an H-counter (52), a subtractor (53), a

comparator (54), and an up-down counter (55), wherein the counter (52) counts pulses from the horizontal start signal and the horizontal image end signal and sends the obtained value to the subtractor (53), which subtracts the horizontal image start count value from the horizontal image end count value wherein the comparator (54) judges whether the number of effective dots meet the standard. The comparator (54) generates judgment signals based on the results of the subtraction, wherein the up-down counter (55) performs, or does not perform, a counting operation based on the judgment signals from the comparator (54). When the total of delay values becomes a predetermined value which is not less than a value corresponding to one sampling clock, the delay data generation unit (62) stops delay control, and sends an instruction to terminate detection of the total of dots to the up-down counter (55) (see column 7, line 45-column 10, line 33). The functionality of the sampling clock control circuit (30) as described refers to the means/circuit for stopping as claimed.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for stopping the frequency adjustment operation based on the number of sampling clocks found in the field, as suggested by Koike, in order to thereby provide an clock generation circuit for a display device which allows the device the capability of generating suitable sampling clocks with respect to a plurality of types of image signals whose respective numbers of horizontal effective dots are known or differ, without causing the user to have to make adjustments through control knobs or keys.

Allowable Subject Matter

4. ***Claims 7 and 8*** are allowed.

Response to Arguments

5. Applicant's arguments with respect to claim 1-8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is (703) 305-0143. The examiner can normally be reached on Monday-Friday 9:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras can be reached on (703) 305-9720. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-2600.

adn/ADN


CHANH NGUYEN
PRIMARY EXAMINER